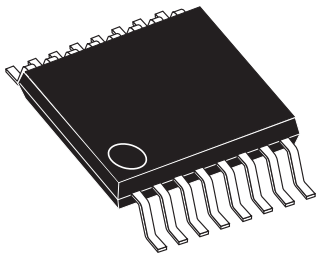
PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMS/15/9519

Analog, MEMS and Sensor Group (AMS)

Additional Back End capacity in Nantong Fujitsu for AMS products in TSSOP16 package



TSSOP16

WHAT:

Progressing on the activities related to TSSOP16 package manufacturing processes expansion, ST is glad to announce an additional production capacity (assembly, test & finishing) for AMS products assembled in TSSOP16 package.
For reference, production in Nantong Fujitsu for AMS is already running since 2008 for Signal conditioning products in TSSOP8 and since 2006 for logic products in TSSOP14/16. This PCN will cover additional products in TSSOP16.

Material	Current process	Modified process
Assembly location	ST Bouskoura (Morocco)	Nantong Fujitsu (China)
Die attach	ABLESTICK 8601S25	ABLEBOND 8200T
Wire	copper 1mils	Gold 1mil
Lead frame	Copper	Copper
Molding compound	SUMITOMO G630AY	Hitachi CEL9210HFVL
Lead finishing	NiPdAgAu	Sn

Samples of test vehicles products are available and other products samples will be available upon request.

WHY:
To increase capacity and improve service to ST Customers for the affected package.

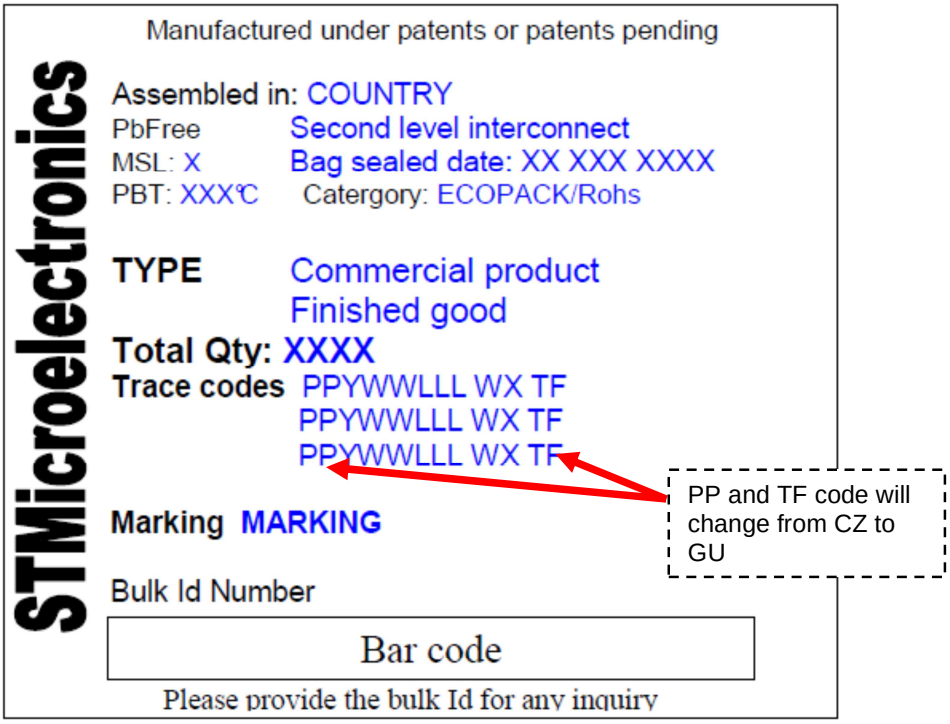
HOW:
The change that covers AMS products packaged in TSSOP16 is qualified through attached qualification plan. Here below you'll find the details of qualification plan.

Qualification program and results:

The qualification program consists mainly of comparative electrical characterization and reliability tests. Please refer to Appendix 1 for all the details.

WHEN:
The production for additional TSSOP16 product from AMS is forecasted in January 2016.
Production in Nantong Fujitsu for AMS group is already running since 2008 for Signal conditioning products in TSSOP8 and since 2006 for Logic products in TSSOP14/16.

Marking and traceability:
Unless otherwise stated by customer specific requirement, the traceability of the parts assembled in Nantong Fujitsu will be ensured by marking on package and on label as per below description:



MSL: Moisture sensitivity level as per Jedec J–std-020C
PBT: Peak body temperature (maximum temperature for reflow soldering)
ECOPACK: present if leadfree component
TYPE: product name
Trace codes: PP: assembly plant code
Y: last digit of the year of assembly
WW: Week of assembly
LL1: lot number
WX: Diffusion plant code
TF : Test&finishing plant code

Bulk ID number: 1: Product level (T for tested product)
Y: last digit of the year
P: Plant code
WW: Week of labeling
LOT: Sequential number for lot
BOXX: Sequential number for box

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.
There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change.
After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
In any case, first shipments may start earlier with customer's written agreement.

Qualification Report

General Information		
Product Line	:	0339, 0464,Z460, E157
Product Description	:	Quad op amps, Logics
Commercial Product	:	LM339PT, TS974IPT, M74HC4060TTR, 74LCX157TTR
Product division/BU	:	Analog and Audio system
Package	:	TSSOP14, TSSOP16
Technology process	:	Bipolar, HF2CMOS, High speed CMOS, HCMOS4
Jedec MSL	:	1

Locations	
Wafer fab location	Ang Mo Kio (singapore) Catania (Italy)
EWS plant location	Toa Payoh (singapore) Catania (Italy)
Final test plant location:	Nantong fujitsu (China)

DOCUMENT APPROVAL LIST

NAME	FUNCTION	DATE	VISA
Jean-Marc Bugnard	Quality Manager AMS Grenoble	28th October 2015	

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

1 RELIABILITY and qualification evaluation overview

1.1 Objectives

The aim of this report is to present the qualification plan of the reliability evaluations performed on TSSOP14 /16 packages produced in Nantong Fujitsu for AMS group.
These results will come in addition to the TSSOP8 signal conditioning and TSSOP14 Logic results as they have been qualified previously (PCN 2242, 8542 and 7092,)

1.2 Conclusion

All results are inside ST specification and the plan to achieve qualification exercise is described in below sections.
TSSOP14/16 is already produced in Nantong Fujitsu since 2006 for Logic products which also belong to the AMS group. The aim of this document is to explain the additional qualification tests performed to add the production of signal conditioning products in TSSOP14/16 in Nantong Fujitsu.

2 DEVICES TRACABILITY

2.1 test vehicle information

	P/N LM2901PT	P/N TS974IPT	P/N M74HC4060TTR	P/N M74HC4060TTR	P/N M74HC4060TTR	P/N 74LCX157TTR
Wafer/Die fab. information						
Wafer fab manufacturing location	AMK6	AMK6	AMJ9	AMJ9	AMJ9	AMK6
Technology	Bipolar	HF2CMOS	High speed CMOS	High speed CMOS	High speed CMOS	HCMOS4
Process family	Bipolar	HF2CMOS	High speed CMOS	High speed CMOS	High speed CMOS	HCMOS4
Die finishing back side	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon	Raw silicon
Die size	1100x1090 µm	1410x1450 µm	2284x1794 µm	2284x1794 µm	2284x1794 µm	996x1176 µm
Bond pad metallization layers	AlSiCu	AlSiCu	AlSi	AlSi	AlSi	AlSiCu
Passivation type	Nitride	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)	P-VAPOX(SiO2) / NITRIDE (SiN)	PSG + Nitride
Wafer Testing (EWS) information						
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K
Assembly information						
Assembly site	NFME	NFME	NFME	NFME	NFME	NFME
Package description	TSSOP14	TSSOP14	TSSOP16	TSSOP16	TSSOP16	TSSOP16
Molding compound	CEL-9210HFVL	CEL-9210HFVL	CEL-9210HFVL	CEL-9210HFVL	CEL-9210HFVL	CEL-9210HFVL
Frame material	Cu	Cu	Cu	Cu	Cu	Cu
Die attach process	Glue	Glue	Glue	Glue	Glue	Glue
Die attach material	Ablestick 8200T	Ablestick 8200T	Ablestick 8200T	Ablestick 8200T	Ablestick 8200T	Ablestick 8200T
Wire bonding process	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding	Thermosonic Ball bonding
Wires bonding materials/diameters	Au 1 mil	Au 1 mil	Au 1 mil	Au 1 mil	Au 1 mil	Au 1 mil
Lead finishing process	preplated	preplated	preplated	preplated	preplated	preplated
Lead finishing/bump solder material	Sn	Sn	Sn	Sn	Sn	Sn
Final testing information						
Testing location	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura	Bouskoura
Tester	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K	ASL1K

3.1 Test vehicle

Lot #	Process/ Package	Product Line
1	Bipolar / TSSOP14	033901
2	HF2CMOS / TSSOP14	0464
3	High speed CMOS / TSSOP16	Z460
4	High speed CMOS / TSSOP16	Z460
5	High speed CMOS / TSSOP16	Z460
6	HCMOS4 / TSSOP16	E157

Detailed results in below chapter will refer to P/N and Lot #.

3.2 Test plan and results summary

Test	PC	Std ref.	Conditions	Steps	Failure/SS					
					Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6
Die Oriented Tests										
HTB	N	JESD22 A-108	Tj = 125°C, BIAS	168 H	0 / 78	/	0 / 18	/	/	0 / 36
				500H	0 / 78	/	0 / 18	/	/	0 / 36
				1000H	0 / 78		0 / 18			0 / 36
HTSL	N	JESD22 A-103	Ta=150°C	168 H			0 / 40	0 / 40	0 / 40	0 / 77
				500H			0 / 40	0 / 40	0 / 40	0 / 77
				1000H			0 / 40	0 / 40	0 / 40	0 / 77
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times	Final	PASS	PASS	PASS	PASS	PASS	PASS
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	96 H	0 / 78	0 / 78				
				168 H			0 / 40	0 / 40	0 / 40	0 / 77
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	100 cy	/	0 / 78	0 / 40	0 / 40	0 / 40	/
				500 cy	/	0 / 78	0 / 40	0 / 40	0 / 40	0 / 77
				1000 cy		0 / 78	0 / 40	0 / 40	0 / 40	
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS	168H	/	/	0 / 140	0 / 100	0 / 100	0 / 36
				1000H						0 / 36

For reference, the below results described the tests done previously for TSSOP14 Logic qualification :

MPA (Micro, Power, Analog) Group
Voltage Regulator, Interface, Advanced logic & Power RF
Quality & Reliability

REL-019W06

Reliability Evaluation Plan and Results on

NANTONG FUJITSU – TSSOP Package

Test	Conditions	S.S.	Requirement	Results
PRECONDITIONING OF SMD DEVICES BEFORE TC/THB/PP	DRYNG 24H @ 125°C STORE 192H @ TA=30°C RH=60% IR 3 times @ Tmax= 260°C		Parameter deviation within spec. limits at end of preconditioning - go no go	No parameter deviation out of spec. limits at end of preconditioning
H.T.S.	TA=150°C	77x3 Lot	Parameter deviation within spec. limits at 1000h	No parameter deviation out of spec. limits at 1000 hours
T.H.B.	*D.U.T. PRECONDITIONED* TA=85°C – RH=85% Vbias	77x3 Lot	Parameter deviation within spec. limits at 1000h	No parameter deviation out of spec. limits at 1000 hours
H.T.B.	TA=125°C – Vbias	77x3 Lot	Parameter deviation within spec. limits at 1000h	No parameter deviation out of spec. limits at 1000 hours
PRESSURE POT	*D.U.T. PRECONDITIONED* TA=121°C – PA=2ATM	77x3 Lot	Parameter deviation within spec. limits at 168h	No parameter deviation out of spec. limits at 168 hours
THERMAL CYCLES AIR TO AIR	*D.U.T. PRECONDITIONED* TA=-65°C TO 150°C 1 HOUR/CYCLE	77x3 Lot	Parameter deviation within spec. limits at 500cycles	No parameter deviation out of spec. limits at 500 cycles
SMD MOISTURE INDUCED STRESS	DRYNG 24H @ 125°C STORE 192H @ TA=30°C RH=60% IR 3 times @ Tmax= 260°C	25x3 Lot	Parameter deviation within spec. limits at end of test	No parameter deviation out of spec. limits at end of test

4 Annexes

4.1 Tests Description

Test name	Description	Purpose
Die Oriented		
HTB High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
Package Oriented		
AC autoclave	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

5 GLOSSARY

ESD	Electro Static Discharge
ELFR	Early Life Failure Rate
GL	Gate Leakage
HTB	High Temperature Bias
HTRB	High Temperature Reverse Bias
HTS	High Temperature Storage
T.H.B.	Temperature Humidity Bias
T.C.	Thermal Cycle
P.P.	Pressure Pot
P.C.	Preconditioning